REMARKS

This is a full and timely response to the outstanding final Office action electronically delivered on December 1, 2010. Reconsideration and allowance of the application and presently pending claims 1-4, 13 and 15 are respectfully requested.

Present Status of the Application

Applicants thank the Examiner for the thorough examination of this application.

In the instant Office action, claims 1-4, 13 and 15 are rejected under 35 U.S.C 103(a) as being unpatentable over Quigley (U.S. Pat. No.5,781,388; hereinafter "Quigley") in view of Lin (U.S. Pat. No.5,982,601; hereinafter "Lin") and Ker et al. (U.S. Pat. No.5,754,380; hereinafter "Ker"). Claims 1-4, 13 and 15 are rejected under 35 U.S.C 103(a) as being unpatentable over Lin in view of Ker.

After carefully considering the Office Action and the cited references, Applicants have amended claim 1 to respectfully traverse all the rejections on the grounds set forth in detail below. No new matter has been entered since the amendment is fully supported by FIGs. 4, 5A, 5B and the related illustration thereof as originally filed. Applicants thereby respectfully assert that all the pending claims 1-4, 13 and 15 are placed in proper condition for allowance. Reconsideration of all the pending claims is respectfully requested.

Interview Summary

Applicants respectively recall during the telephone interview conducted between our Attorney of record Mr. Michael Su and the Examiner NADAV, ORI. Examiner NADAV, ORI suggested an amendment to claim 1, which will overcome the rejection, as recited in previous office action.

Discussion of the claim rejection under 35 USC 103

Claims 1-4, 13 and 15 are rejected under 35 U.S.C 103(a) as being unpatentable over Quigley in view of Lin and Ker et al. Claims 1-4, 13 and 15 are rejected under 35 U.S.C 103(a) as being unpatentable over Lin in view of Ker.

In response thereto, Applicants have amended claim 1 to patently define the present application over the cited references Quigley, Lin and Ker. Now, Applicants hereby otherwise traverse these rejections.

Pertaining to claim 1 of the present invention, as currently amended, it recites in part as below:

"An electrostatic discharge (ESD) protection circuit, comprising:

...

a first diode, having a first input end coupled to the I/O pad and a second input end coupled to the fourth connection terminal, wherein **when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-**

latch-up circuit does not substantially generate the anti-latch-up signal." *(Emphasis added)*

Referring to FIG. 6B and column 4 of Lin, it recites in part as below:

"….the gate of M2 remains at a much lower voltage than the threshold voltage required to turn on M2. Therefore, the oscillator circuit does not oscillates during normal IC operation or powering up…." (*Emphasis added*)

It can be know that, during normal IC operation or powering up, the transient oscillator circuit 61 does not oscillate, so that the transient oscillator circuit 61 at these moments is incapable of providing a high voltage to the n-well of the SCR. In other words, during normal IC operation or powering up, the transient oscillator circuit 61 is incapable of providing an anti-latch-up signal for the SCR.

In contrast, referring to FIGs. 4, 5A, 5B and the related illustration of the present invention, when the IC is powering up, the diode 108 is in a non-conducting state. The anti-latch-up circuit 110 is hence able to generate an anti-latch-up signal by according to the power voltage Vcc, so as to prevent latch-up of the SCR circuit 104. In other words, when the diode 108 is in a non-conducting state (i.e. during normal IC operation or powering up), the anti-latch-up circuit 110 is able to generate an anti-latch-up signal.

In short, during normal IC operation or powering up, the transient oscillator circuit 61 of Lin does not generate a signal to prevent latch-up of the SCR, whereas in the claimed invention, when the IC is powering up, the diode 108 is in a non-conducting state, so that the anti-latch-up circuit 110 generates an anti-latch-up signal.

Furthermore, Applicants would like to point out that even if Lin and Kerr were combined, they do not collectively teach the synergistic relationship between the claimed anti-latch-up

circuit 110 and the diode 108. In the claimed invention, the claimed anti-latch-up circuit 110 operates according to whether the diode 108 is in a non-conducting state. The Office, however, asserts that these two claimed elements are respectively equivalent to the transient oscillating circuit 61 of Lin and the diode 60 of Kerr. However, none of the cited references teaches operating the transient oscillating circuit 61 according to the state of a diode.

Besides, Applicants submit that the transient oscillating circuit 61 of Lin and the diode 60 of Kerr cannot be combined. Referring to Fig. 1 and column 5 of Kerr, it recited in part as cited below:

"….The D_p diode 60 to is used to bypass the PD-mode ESD stress….." (*Emphasis added*)

It can be known that the diode 60 of Kerr is used to bypass the ESD stress to the VDD bus.

On the other hand, referring to column 2 of Lin, it cited in part as below:

"….A transient voltage oscillation circuit is coupled to the first region for forward-biasing the junction at the second region and the first region (P+/nwell junction) at least once during the ESD event for earlier triggering said SCR during the ESD event. The present invention improves the ESD performance of an SCR ESD protection circuit which is used for protecting the power bus or an IC pin during an ESD event." (*Emphasis added*)

It is clear that the transient oscillator circuit 61 of Lin is used to trigger the SCR during the ESD event, so that the SCR can conduct a greater current to ground, thereby protecting the power bus. This is the opposite of Kerr, which teaches to conduct the ESD stress to the VDD bus. Therefore, it is submitted that Lin and Kerr cannot be combined by one of ordinary skill in the art to obtain the claimed invention.

"[O]bviousness requires a suggestion of all limitations in a claim." *CFMT, Inc. v. Yieldup Int'l. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (citing *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)).

From the above, neither Quigley nor Lin teaches at least the feature of the claimed anti-latch-up circuit and the claimed first diode recited in the amended claim 1, "wherein when the first diode is not conducted, the anti-latch-up circuit substantially generates an anti-latch-up signal to the third connection terminal of the SCR circuit according to the voltage source so as to prevent latching up of the SCR circuit during normal operation, and when the first diode is conducted, the anti-latch-up circuit does not substantially generate the anti-latch-up signal." Moreover, Ker is also deficient in teaching said feature. Therefore, the teachings of Quigley, Lin, and Ker, in any combination, fail to render the invention set forth in claim 1 obvious. Applicants respectfully submit that claim 1 is patentable and allowable over the cited references.

If an independent claim is non-obvious under 35 U.S.C. 103, then any claim depending therefrom is non-obvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). As a result, claims 2-4, 13 and 15 directly or indirectly depending upon the allowable claim 1 should be allowed as a matter of law.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-4, 13 and 15 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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/JIAWEI HUANG/
Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809
Email: jcpi@msn.com